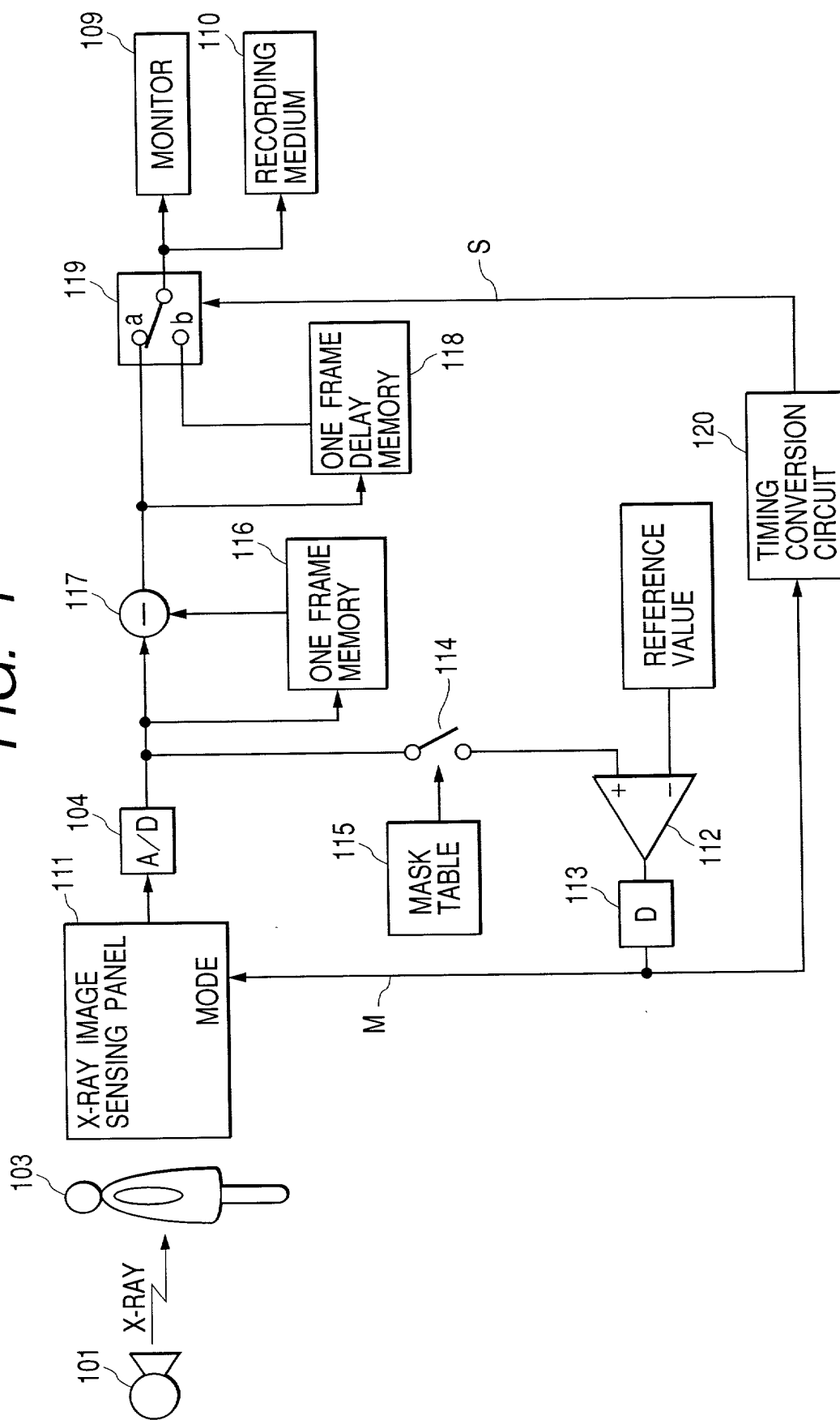
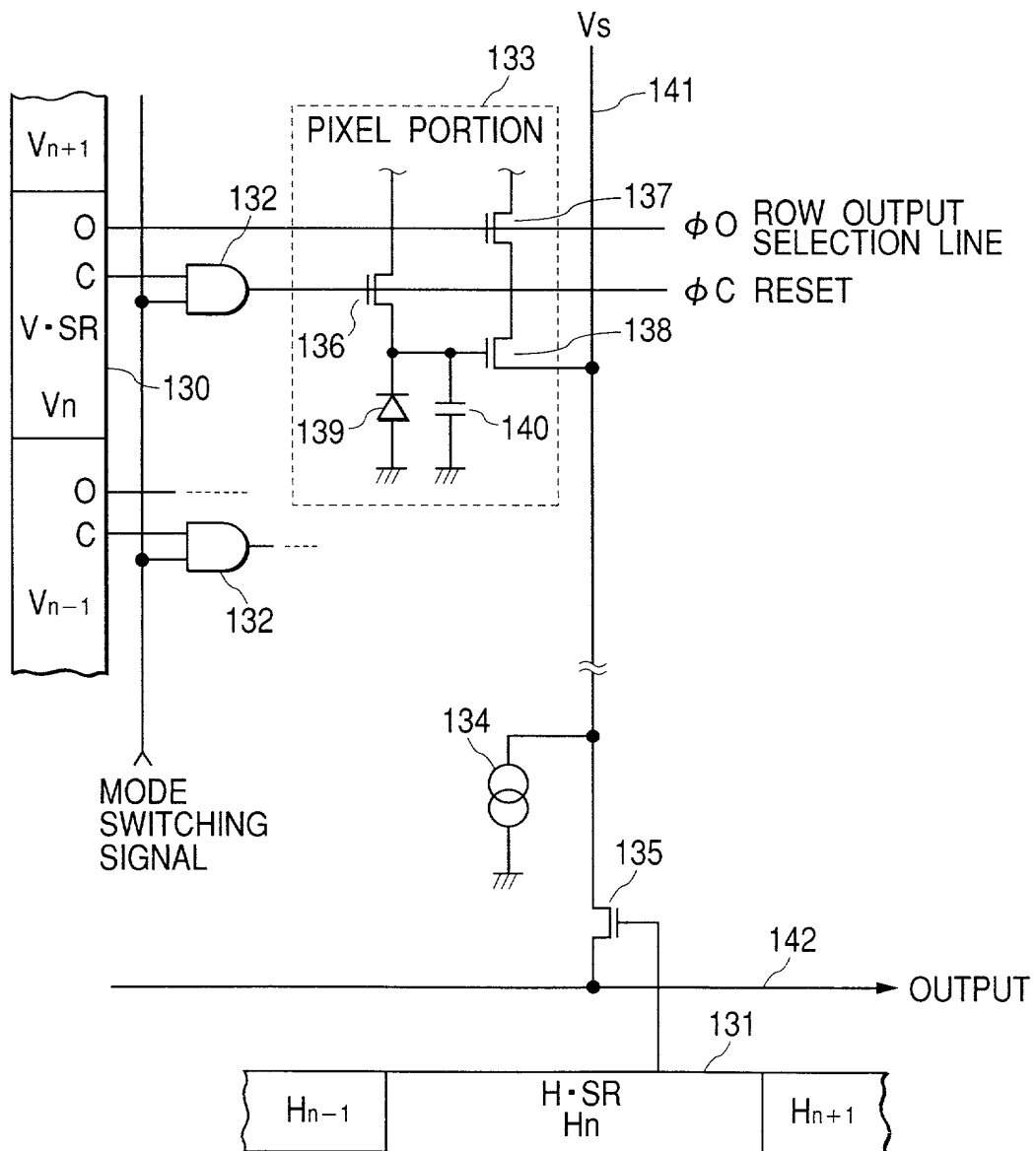
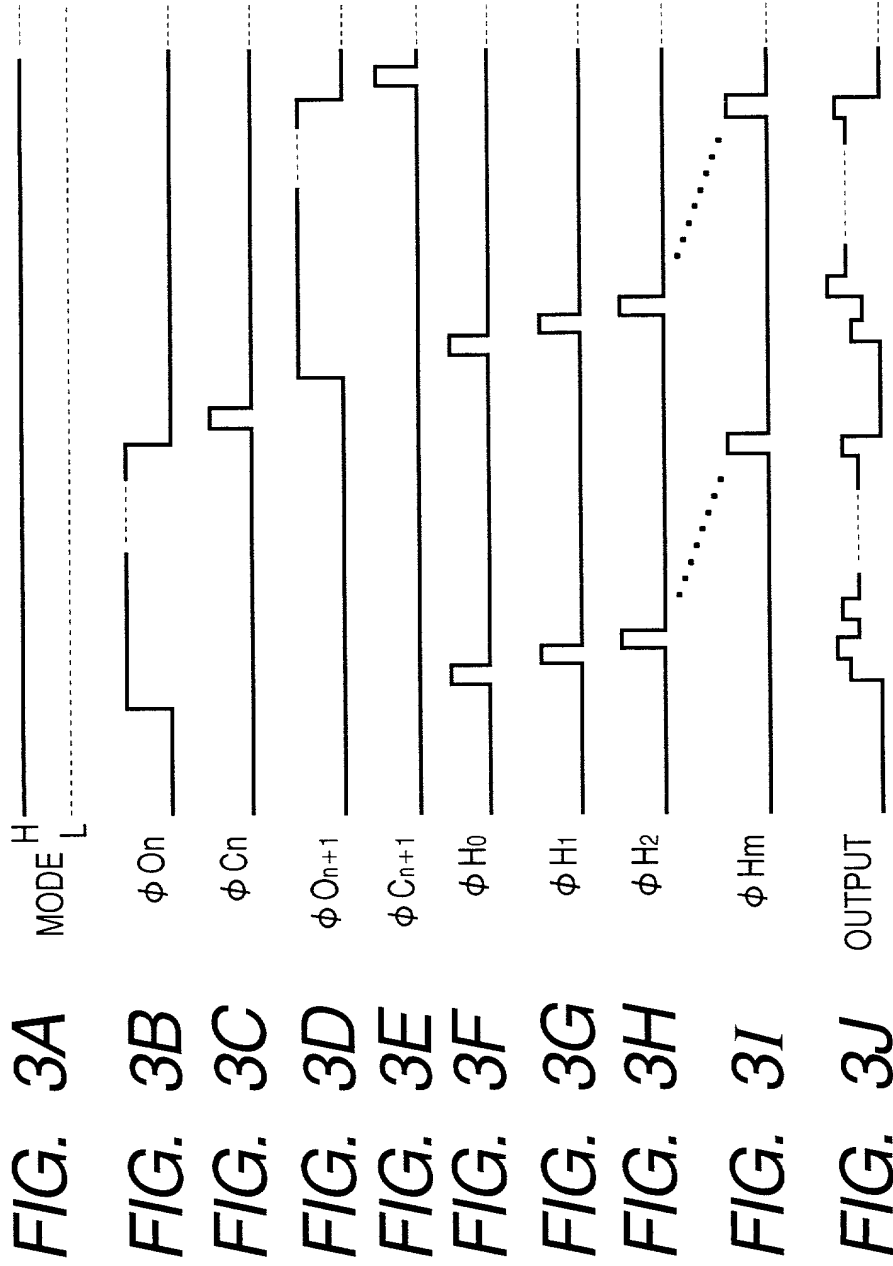


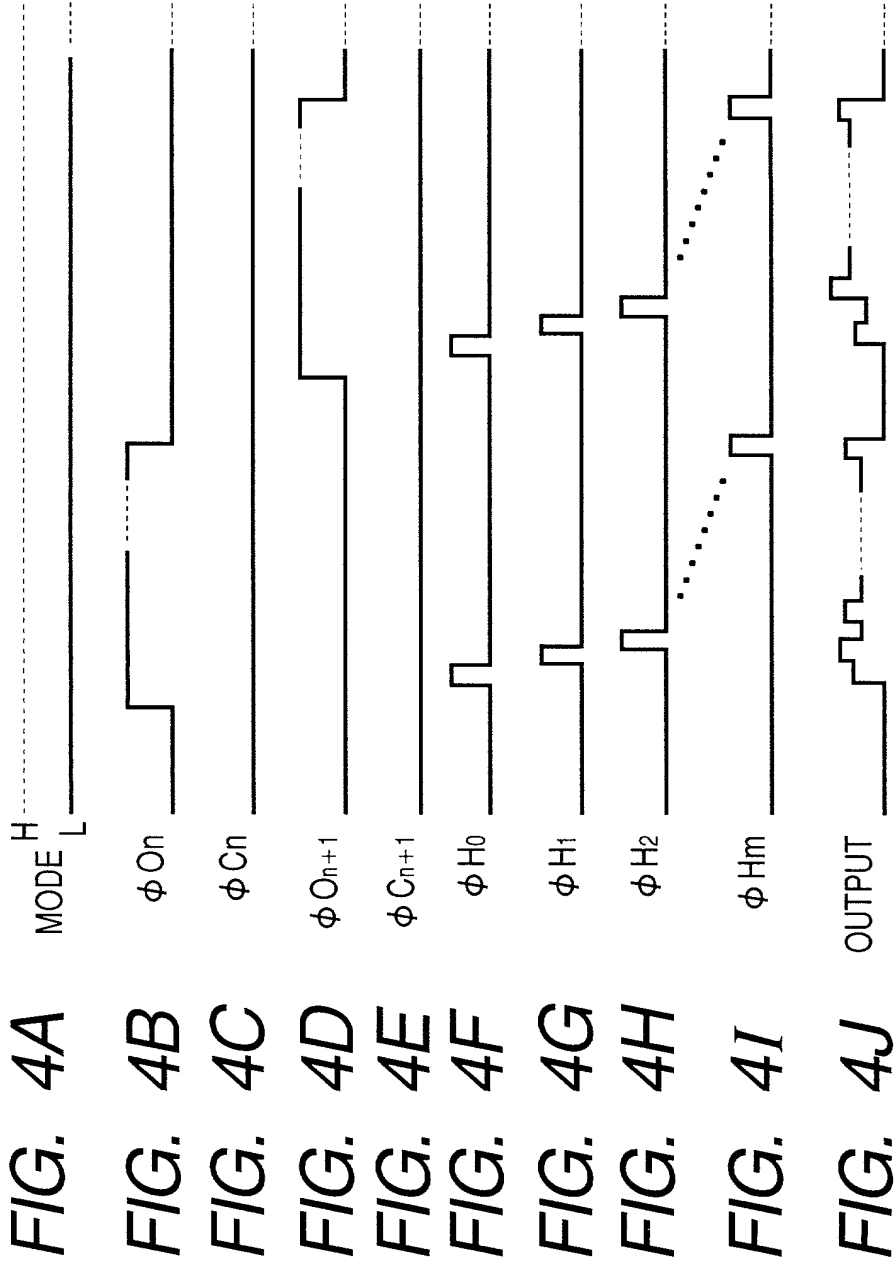
FIG. 1



**FIG. 2**







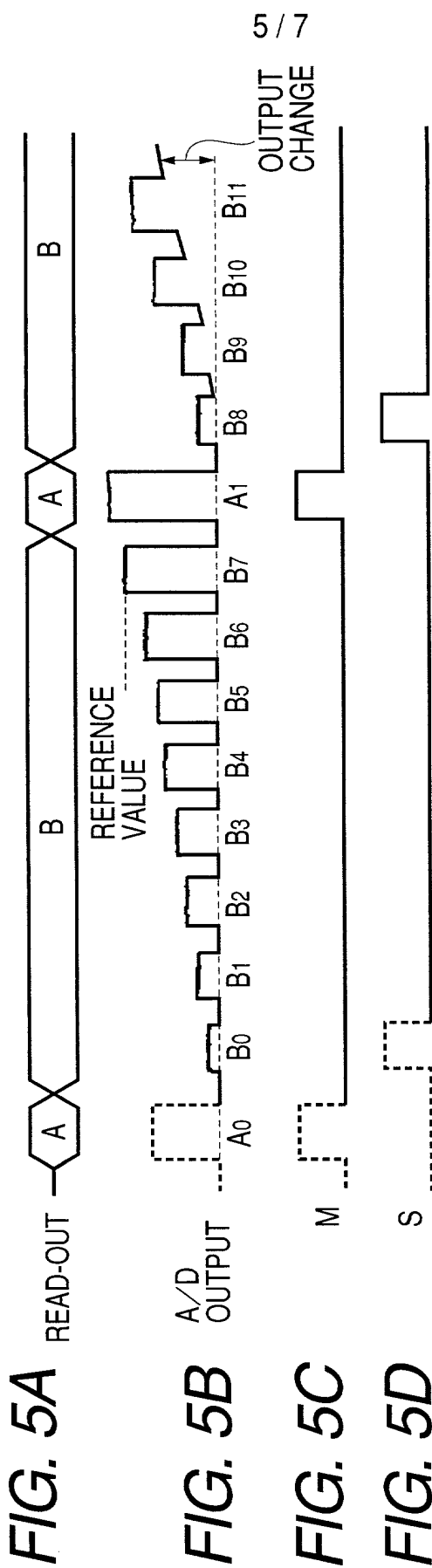


FIG. 6

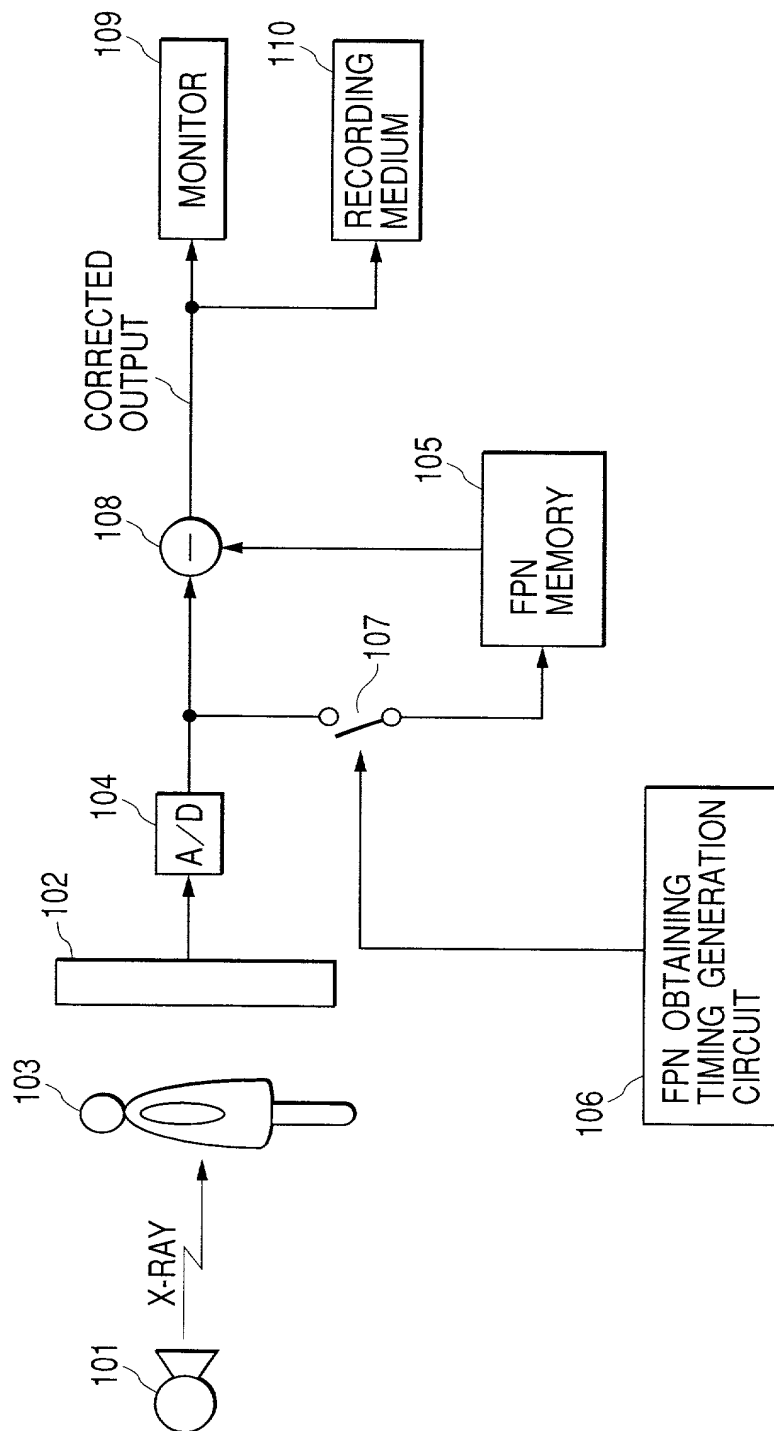


FIG. 7A FPN OBTAINING  
TIMING SIGNAL



FIG. 7B A/D  
OUTPUT



FIG. 7C CORRECTED  
OUTPUT

